## REMARKS

In light of the foregoing remarks and amendments set forth herein, reconsideration and withdrawal of the objection and the rejections set forth in the Office Action dated November 12, 2004 are respectfully requested. Claims 1-12 were pending in this application at the time the present Office Action was mailed. In the Office Action, the Examiner objected to the drawings and rejected claims 1-12. Claims 1 and 7 have been amended in this correspondence; accordingly, claims 1-12 are now pending. Further, in light of the amendments to the claims, applicant respectfully submits that corrections to the drawings are not necessary.

Claims 1, 2 and 4-6, including independent claim 1, were rejected under 35 U.S.C. § 102(b) as being anticipated by Inoue et al. ("Inoue") U.S. Patent No. 6,211,509. In short, the Office Action argued that Inoue illustrates a similar semiconductor circuit, wherein the amplification transistor is a buried transistor. Applicant acknowledges that Inoue does teach a four transistor CMOS pixel, such as that illustrated in the present specification in Figures 1 and 2.

However, the key to the present claimed invention is that **the amplification transistor is a "body current" device**. See paragraphs 14-15, pages 3-4. In other words, most of the current flowing through the amplification transistor is not at the surface as is the case with conventional transistors. Applicant has recognized that current that flows at the surface, surface oxide traps can be avoided and 1/f flicker noise can be reduced.

The Examiner asserts that amplification transistor 23 of Inoue is a "buried transistor". This is simply not the case. Applicant has thoroughly reviewed the Inoue patent and can find no reference that amplification transistor 23 is a buried transistor where most of the current flows through the body of the transistor. The Examiner is respectfully requested to point out with particularity the portions of Inoue that state that the amplification transistor 23 is a buried or body current transistor. Further, in the interest of

clarity, applicant has amended Claim 1 to state that the amplification transistor is a body current transistor where most of the current flows through the body of the transistor.

Claims 7-12, including the independent claim 7, were rejected under 35 U.S.C. § 102(b) as being anticipated by Matsunaga et al. ("Matsunaga") U.S. Patent No. 6,239,839. Like above, the Examiner argues that Matsunaga illustrates a similar semiconductor circuit, wherein the amplification transistor is a body current transistor. Applicant acknowledges that Matsunage teaches a CMOS image sensor.

However, as noted above, the key to the present claimed invention is that **the amplification transistor in the pixel is a "body current" device**. See paragraphs 14-15, pages 3-4. In other words, most of the current flowing through the amplification transistor is not at the surface as is the case with conventional transistors. Applicant has recognized that current that flows at the surface, surface oxide traps can be avoided and 1/f flicker noise can be reduced.

The Examiner asserts that amplification transistor 64 of Matsunaga is a "buried transistor". This is simply not the case. The amplification transistor 64 of Matsunaga is a conventional surface current transistor. The Examiner is respectfully requested to point out with particularity the portions of Matsunaga that state that the amplification transistor 23 is a buried or body current transistor. Further, in the interest of clarity, applicant has amended Claim 1 to state that the amplification transistor is a body current transistor where most of the current flows through the body of the transistor.

In addition, neither of the references cited in the Office Action attempts to solve the problem being solved by the present invention. The cited references do not even address the problem. Therefore, in light of the above arguments, a *prima facie* case of anticipation under Section 102 has not been established with regard to claims 1 and 7; hence, the undersigned respectfully requests the withdrawal of the respective rejections.

Claims 2 and 4-6 depend from claim 1 and claims 8-12 depend from claim 7 and hence include the features of claims 1 and 7, respectively. For reasons discussed above and for the additional features of these claims, a *prima facie* case of anticipation under Section 102 has not been established with respect to these claims and accordingly the Section 102 rejection of claims 2, 4-6, and 8-12 should be withdrawn.

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Inoue as applied to claim 1 above, and further in view of Matsunaga. Claim 3 depends from claim 1 and hence includes the features of claims 1. For reasons discussed above and for the additional features of this claim, a *prima facie* case of obviousness under Section 103 has not been established with respect to this claim and accordingly the Section 103 rejection of claim 3 should be withdrawn.

In view of the foregoing, all of the claims pending in the application are in condition for allowance and, therefore, a Notice of Allowance is respectfully requested. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-6488. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 386168009US from which the undersigned is authorized to draw.

Dated: 1/12/05

Respectfully submitted,

By _____

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